REMARKS

Prior to entry of the present amendment, claims 54-56 and 65-114 were pending in the present application. Claims 72 and 81-86 are withdrawn above. Claims 54, 65, 66, 77, 78, 79, 80, 87, 91, 93, 106, 110 and 112 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 54-56 and 65 stand rejected under 35 U.S.C. 112, first paragraph. The Office Action states at page 3, paragraph 1, that Applicant did not disclose "a second clock generator independent of both the controller and the memory module for generating a second clock signal" in the original disclosure. The Applicant respectfully disagrees. It is noted that the "second clock generator independent of both the controller and the memory module for generating a second clock signal" is described in the specification as filed at least at page 9, lines 19-21 and page 16, lines 3-21, and at FIG. 9 of the drawings. Accordingly, reconsideration and removal of the rejection are respectfully requested.

Claims 66-90 and 106-109 stand rejected under 35 U.S.C. 112, second paragraph. Claims 66 and 106 are amended above to recite "a control/address buffer device". It is believed that the claims are amended above in a manner to address and overcome the rejections. Entry of the amendments and reconsideration and removal of the rejections are respectfully requested.

Claims 54-56, 65-67, 73-79, 91, 93-96, 101-104, 106, 107, 109, 110 and 112-114 stands rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* (U.S. Patent Number 6,510,503). Claims 68, 97 and 108 stand rejected under 35 U.S.C.103(a) as being unpatentable over Gillingham, *et al.*, in view of Wada, *et al.* (U.S. Patent Number 5,379,248). Claims 69-71, 87-89 and 98-100 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Yoshitake (U.S. Patent Number 6,043,704). Claims 80, 92 and 111 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Moyal, *et al.* (U.S. Patent Number 6,326,853). Claims 90 and 105 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth (U.S. Patent Number 6,029,250). Reconsideration of the rejection and allowance of the claims are respectfully requested.

In the present invention as claimed in independent claim 54, a memory system having a stub configuration includes a controller for generating a first clock signal, a memory module including memory devices coupled to the controller via a system bus, and a second clock signal generator independent of both the controller and the memory module for generating a second clock signal independently from the first clock signal that is sourced at a location that is beyond an outermost memory module on the system bus relative to the controller. The memory module receives the first clock signal and the second clock signal.

In the present invention as claimed in independent claim 65, a method of transferring data in a memory system having a stub configuration includes generating a first clock signal at a controller, and generating a second clock signal independently from the first clock signal at a second clock signal generator independent of both the controller and a memory module including memory devices coupled to the controller via a system bus such that the second clock signal is sourced at a location that is beyond an outermost memory module on the system bus relative to the controller. The method further includes receiving the first clock signal and the second clock signal at the memory module.

With regard to the rejection of claim 54, Gillingham, *et al.* fails to teach or suggest a memory system that includes "a controller for generating a first clock signal", "a memory module including memory devices coupled to the controller via the system bus", and a "second clock signal generator independent of both the controller and the memory module for generating a second clock signal independently from the first clock signal that is sourced at a location that is beyond an outermost memory module on the system bus relative to the controller". Instead, in Gillingham, *et al.*, the outclk signal is a delayed signal of the clock 86, CLK (referred to in the Office Action as being analogous to applicants' "first clock"), and the delayed CLK signal outclk drives the data clock signal dclk (outclk and dclk are referred to in the Office Action as being analogous to applicants' "second clock"). Therefore, the outclk and the dclk signals are not generated "independently from" the clock signal 86, CLK. In addition, the fine vernier delays 107 and 108 of Gillingham, *et al.* are within a memory device interface circuit and therefore

the outclk signals generated by the fine vernier delays 107 and 108 are not "sourced at a location that is beyond an outermost memory module on the system bus relative to the controller", as claimed in claim 54.

With regard to the rejection of claim 65, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system that includes "generating a second clock signal independently from the first clock signal at a second clock signal generator independent" of "both" a "controller" and a "memory module" "such that the second clock signal is sourced at a location that is beyond an outermost memory module on the system bus relative to the controller". Instead, in Gillingham, *et al.*, the outclk signal is a delayed signal of the clock 86, CLK (referred to in the Office Action as being analogous to applicants' "first clock"), and the delayed CLK signal outclk drives the data clock signal dclk (outclk and dclk are referred to in the Office Action as being analogous to applicants' "second clock"). Therefore, the outclk and the dclk signals are not generated "independently from" the clock signal 86, CLK. In addition, the fine vernier delays 107 and 108 of Gillingham, *et al.* are within a memory device interface circuit and therefore the outclk signals generated by the fine vernier delays 107 and 108 are not "sourced at a location that is beyond an outermost memory module on the system bus relative to the controller", as claimed in claim 65.

In the present invention as claimed in claim 66, a memory system having a stub configuration includes a first memory module including at least one memory device connected to a data bus and a first clock signal line for receiving data signals and a first clock signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal.

In the present invention as claimed in claim 91, a memory system having a stub configuration includes a first memory module including at least one memory device connected to a data bus and a first clock signal line for receiving data signals and a first

clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal.

In the present invention as claimed in claim 106, a method of transferring data in a memory system having a stub configuration includes receiving data signals and a first clock signal at a first memory module including at least one memory device connected to a data bus and a first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal at a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line respectively.

In the present invention as claimed in claim 110, a method of transferring data in a memory system having a stub configuration includes receiving data signals and a first clock signal at a first memory module including at least one memory device connected to a data bus and a first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal, at a control/address buffer device.

Gillingham, *et al.*, in FIG. 8(a) discloses a memory device interface circuit that is an input circuit included in a memory device. A command and data interface 98 of the memory device interface includes a first set of programmable delay circuits 102 and 104 for delaying both the rising and falling edges of the received clock signal CLK thereby providing even clock CLK_E and odd clock CLK_O signals which latch even and odd row commands row_E, row_O as well as even and odd column commands col_E, col_O into the core DRAM via D-type flip-flops 106. Separate programmable fine vernier delays 107 and 108 receive as inputs the clock signal CLK and delay the rising and

falling edges to generate delayed signals OUTCLKE and OUTCLKO. These signals drive the clock input of respective D-type latches 120 and 122 for latching the even Data_Out_E and odd Data_Out_O output data signals from the core DRAM. The data input to the memory is synchronized with data clocks dclk0 and dclk1. In this manner, Gillingham, *et al.* teaches that each memory device interface circuit is responsible for transferring signals to and from a single, corresponding, memory device 84, 100 in the memory system. Therefore each memory device 84, 100 in Gillingham, *et al.* includes such a memory device interface circuit and, as a result, each memory device in the memory system of Gillingham, *et al.* will place a load on associated row/column signal lines of the Gillingham, *et al.* system bus (asserted in the Office Action as being analogous to the control/address signals of the present invention).

With regard to claim 66, Gillingham, *et al.* fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed. In Gillingham, *et al.*, the memory device interface circuit is an interface that is included in each memory device on the memory module. In contrast, the control/address buffer device as claimed in claim 66 is included in the "first memory module" and services any or all of the at least one memory devices on the module by supplying the "control signal and the address signal" to each of the "at least one memory device" on the module "in response to the first clock signal", as claimed. By sharing the resources of the control/address buffer device, excessive loading of the "control/address signals" on the system bus is alleviated, and operation speed of the memory system is improved.

With regard to the claim 91, Gillingham, *et al.* further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal

line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed. In Gillingham, *et al.*, the memory device interface circuit is an interface that is included in each memory device on the memory module. In contrast, the control/address buffer device as claimed in claim 91 is included in the "first memory module" and services any or all of the at least one memory devices on the module by supplying the "control signal and the address signal" to each of the "at least one memory device" on the module "in response to the first clock signal" as claimed. By sharing the resources of the control/address buffer device, excessive loading of the "control/address signals" on the system bus is alleviated, and operation speed of the memory system is improved.

With regard to claim 106, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including at least one memory device connected to the data bus and the first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal at a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line respectively", as claimed. In Gillingham, *et al.*, the memory device interface circuit is an interface that is included in each memory device on the memory module. In contrast, the control/address buffer device as claimed in claim 106 is included in the "first memory module" and services any or all of the at least one memory devices on the module by supplying the "control signal and the address signal" to each of the "at least one memory device" on the module "in response to the first clock signal", as claimed. By sharing the resources of the control/address buffer device, excessive loading of the "control/address signals" on the system bus is alleviated, and operation speed of the memory system is improved.

With regard to claim 110, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including at least one memory device connected to the data bus and the first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal, at a control/address buffer device", as claimed. In Gillingham, *et al.*, the memory device interface circuit is an interface that is included in each memory device on the memory module. In contrast, the control/address buffer device as claimed in claim 110 is included in the "first memory module" and services any or all of the at least one memory devices on the module by supplying the "control signal and the address signal" to each of the "at least one memory device" on the module "in response to the first clock signal", as claimed. By sharing the resources of the control/address buffer device, excessive loading of the "control/address signals" on the system bus is alleviated, and operation speed of the memory system is improved.

Accordingly, reconsideration and removal of the rejection of independent claims 54, 65, 66, 91, 106 and 110 under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* are therefore respectfully requested. With regard to the dependent claims 55-56, 67, 73-79, 93-96, 101-104, 107, 109 and 112-114, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejections of claims 68, 97 and 108, Wada, *et al.* is cited in the Office Action as disclosing a memory system wherein first and second signal lines are crossed on the motherboard between the first and second modules.

Like Gillingham, *et al.*, Wada, *et al.* fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock

signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 68. Like Gillingham, *et al.*, Wada, *et al.* further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 97. In addition, like Gillingham, *et al.*, Wada, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including at least one memory device connected to the data bus and the first clock signal line respectively, and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal at a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line respectively", as claimed in claim 108.

Neither Gillingham, *et al.* nor Wada, *et al.* teaches or suggests the present invention as claimed in claims 68, 97 and 108. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Wada, *et al.* fails to teach or suggest the invention as claimed in claims 68, 97 and 108. Reconsideration of the rejection of, and allowance of claims 68, 97 and 108 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Wada, *et al.* are respectfully requested.

With regard to the rejection of claims 69-71, 87-89, 98-100, like Gillingham, *et al.*, Yoshitake fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock

signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 69-71 and 87-89. Like Gillingham, *et al.*, Yoshitake further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 98-100.

Neither Gillingham, *et al.* nor Yoshitake teaches or suggests the present invention as claimed in claims 69-71, 87-89 and 98-100. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Yoshitake fails to teach or suggest the invention as claimed in claims 69-71, 87-89 and 98-100. Reconsideration of the rejection of and allowance of claims 69-71, 87-89 and 98-100 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Yoshitake are respectfully requested.

With regard to the rejections of claims 80, 92 and 111, like Gillingham, *et al.*, Moyal, *et al.* fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 80. Like Gillingham, *et al.*, Moyal, *et al.* further fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the

first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 92. In addition, like Gillingham, *et al.*, Moyal, *et al.* fails to teach or suggest a method of transferring data in a memory system having a stub configuration that includes "receiving the data signals and the first clock signal at a first memory module including at least one memory device connected to the data bus and the first clock signal line respectively, and receiving the first clock signal at a clock return that is coupled to the first clock signal line and receiving the control signal, the address signal, and the first clock signal and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal, at a control/address buffer device", as claimed in claim 111.

Neither Gillingham, *et al.* nor Moyal, *et al.* teaches or suggests the present invention as claimed in claims 80, 92 and 111. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Moyal, *et al.* fails to teach or suggest the invention as claimed in claims 80, 92 and 111. Reconsideration of the rejection of, and allowance of claims 80, 92 and 111 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Moyal, *et al.* are respectfully requested.

With regard to the rejection of claims 90 and 105, like Gillingham, *et al.*, Keeth fails to teach or suggest a memory system having a stub configuration that includes "a first memory module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a control/address buffer device that is connected to the control signal line, the address signal line and the first clock signal line for receiving the control signal, the address signal, and the first clock signal respectively and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 90. Like Gillingham, *et al.*, Keeth further fails to teach or suggest a memory system having a stub configuration that includes "a first memory

module including at least one memory device connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return that is coupled to the first clock signal line that receives the first clock signal, and a control/address buffer device receiving the control signal, the address signal, and the first clock signal respectively, and supplying the control signal and the address signal to the at least one memory device in response to the first clock signal", as claimed in claim 105.

Neither Gillingham, *et al.* nor Keeth teaches or suggests the present invention as claimed in claims 90 and 105. Accordingly, it is submitted that the combination of Gillingham, *et al.* and Keeth fails to teach or suggest the invention as claimed in claims 90 and 105. Reconsideration of the rejection of, and allowance of claims 90 and 105 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Keeth are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: December 21, 2006

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